REMARKS

Reconsideration and allowance are requested.

Applicant notes with appreciation the indication of allowable subject matter in claim 11. Claim 11 has been amended to depend from claim 1, and new claim 20 depending from claim 19 has been added which includes the allowable subject matter of claim 11.

Most of the claims stand rejected for anticipation based U.S. patent 6,018,624 to Baxter. This rejection is respectfully traversed.

To establish that a claim is anticipated, the Examiner must point out where each and every limitation in the claim is found in a single prior art reference. *Scripps Clinic & Research Found. v. Genentec, Inc.*, 927 F.2d 1565 (Fed. Cir. 1991). Every limitation contained in the claims must be present in the reference, and if even one limitation is missing from the reference, then it does not anticipate the claim. *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565 (Fed. Cir. 1986). Baxter fails to satisfy this rigorous standard.

Baxter discloses a simulation model for a new target technology integrated circuit implementation (e.g., a MPIC) of a circuit design from a programmable logic device (PLD) (e.g., a FPGA) simulation model for that same circuit design. The designer begins with the simulation model of the PLD and "back annotates" the simulation model with timing characteristics from a target technology. The back annotation substitutes timing values in the PLD simulation model with timing values from the target technology to generate the new integrated circuit simulation model. The timing values include three types of delays: specification delays, derived delays and net delays. Each of these delays corresponds to various logic elements used to perform desired functions. Although the PLD implements the functions differently than the new integrated circuit, the functions are the same.

The model of the PLD device, which includes timing information, is modified to form a model of the target device. This modification is carried out, not by performing an analysis of the target device, but rather by a component matching technique using a set of timing data calculated for the generic implementation technology of the target device. More particularly, a library of functional components and their delays is generated for the particular target technology. This library specifies a delay associated with each of those functional elements, or a way in which that delay may be simply calculated, (e.g., a net delay corresponding to propagation of a signal along a wire). The PLD model is broken down into its functional model elements (see step 220 of Figure 2). The delay for each of those model elements is retrieved from the library for the target implementation and substituted into the original PLD model in place of the delay value corresponding to the PLD implementation.

Baxter's technique is based upon matching functional model elements and directly substituting the original delay from the PLD model with a delay for the same functional model element in the target technology library. But this technique does not disclose the features recited in independent claims 1 and 19. For example, Baxter fails to teach the claim feature "calculating signal delays for signal transitions within said circuit component model using a delay calculator *and* a *subset* of said set of associated delays and rules" recited in claim 1. The Examiner refers to column 2, line 41 to column 3, line 13. But this text fails to teach using a subset of the set of associated delays and rules for the given implementation of the IC. The use of a subset is significant because it is not practical to use all of the associated delays and rules for the given implementation of the IC in delay calculations.

Baxter also lacks the searching claim feature of claim 1: "searching said circuit component model to identify *signal transitions* corresponding to signal transitions with

associated signal delays as calculated by said delay calculator." As explained above, Baxter searches for matching functional model elements rather than searching for *signal transitions* corresponding to signal transitions with associated signal delays as calculated by the delay calculator.

Baxter further lacks the claimed modifying step in which the identified matching transitions are modified using the delays calculated by the delay calculator *and* the set of associated delays and rules (which are the same as those referred to in the first element of the claim). Although Baxter does do some matching and modification, Baxter matches a different thing and modifies it in a different way using different information than what is claimed.

Claims 1 and 19 form a model with a set of delays and rules for a given implementation and calculate signal delays for signal transitions using a subset of those rules in a manner that makes the delay calculation practical (i.e., the delays have not been calculated for all conditions). The model is searched for signal transitions for which a delay has been calculated and then the set of associated delays and rules from the originally form of the model are used to augment the calculated delays and to modify the model with now more comprehensive delay information. While there is a coincidence of similar words like searching, matching, annotation, etc., Baxter's approach is quite different to that claimed. Baxter is concerned with forming a new model for a new device by reusing an old model for an different, but functionally equivalent device and substituting delay values in the old model with delay values for corresponding functional model elements within the new implementation/model.

The application is in condition for allowance. An early notice to that effect is earnestly solicited.

Respectfully submitted,

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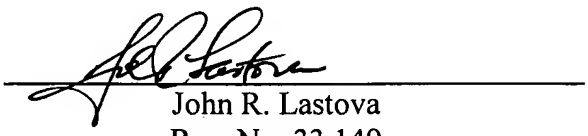
By: 
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